IN THE SPECIFICATION

Please add the following to the Reference to Prior Application on page 1, lines 4-5:

-- This application is a continuation of U.S. Patent Application Serial No. 09/877,793, which issued as U.S. Patent No. 6,668,308 by L.A. Barroso et al. on December 23, 2003, and is entitled "Scalable Architecture Based on Single-Chip Multiprocessing." --

Please amend the Cross Reference to Related Application on page 1, lines 8-10, as follows:

~~-- This application is related to and incorporates herein by reference U.S. Patent Application Serial No. 10/210,655, filed June 9, 2002, by L. A. Barroso et al. entitled "Method and System for Exclusive Two-Level Caching in a Chip-Multiprocessor."~~

This application is related to and incorporates herein by reference U.S. Patent Application Serial No. 09/877,530, which was filed on June 8, 2001, by L.A. Barroso et al., entitled "Method and System For Exclusive Two-Level Caching in a Chip-Multiprocessor." --